In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Canceled)

2. (Currently Amended) A computer implemented method of rasterizing a page in a page description language in a multiprocessor integrated circuit comprising the steps of:

interpreting said page in said page description language with a first processor of said multiprocessor integrated circuit;

spawning a subtask from said first processor to another of said processors for sorting polygon edges in increasing minimum Y coordinate, wherein each of said other processors is a digital signal processor having an integer multiplier unit; and

spawning a subtask from said first processor to another of said processors for detecting a Y coordinate of edge intersection determined to occur between Y coordinates Ytop and Ybottom via successive midpoint approximation by repeatedly

calculating a difference in the X coordinates of the respective edges at Ytop and Ybottom are computed by

$$x1step = X1 - x1$$
$$x2step = X2 - x2$$

where: x1 and x2 are respective X coordinates of two edges at Ybottom; and X1 and X2 are respective X coordinates of said two edges at Ytop,

calculating the X coordinates of the respective edges at Y coordinate Y = (y1+y2)/2 by

$$X1 = (x1 + x1step)/2$$

X2 = (x2 + x2step)/2

setting Ybottom as (Y + Ybottom)/2 if X2 ≥ X1 at Y, and setting Ytop as (Y+Ytop)/2 if X2 ≤ X1, and until a Y coordinate of the intersection point is obtained with a desired accuracy.

3 and 4. (Canceled)

5. (Currently Amended) ~~The~~ A computer implemented method ~~of claim 2,~~ of rasterizing a page in a page description language in a multiprocessor integrated circuit comprising the steps of:

interpreting said page in said page description language with a first processor of said multiprocessor integrated circuit, wherein said first processor is a reduced instruction set processor having a floating point computation unit ~~and said method further comprising:~~;

spawning a subtask from said first processor to another of said processors for sorting polygon edges in increasing minimum Y coordinate; and

calculating a Y coordinate of edge intersection employing said floating point calculation unit of said first processor by

Y = (c1-c2)/(b2-b1)

where: a first edge has vertices (X1,Y1) and (X2,Y2) with b1 = X1 - X2 and c1 = X2*Y1 - X1*Y2; and a second edge has vertices (X3,Y3) and (X4,Y4) with b2 = X3 - X4 and c2 = X4*Y3 - X3*Y4.

6 to 10. (Canceled)

11. (Currently Amended) ~~The~~ A computer implemented method ~~of claim 2,~~ of rasterizing a page in a page description language in a multiprocessor integrated circuit, comprising the steps of:

interpreting said page in said page description language with a first processor of said multiprocessor integrated circuit, wherein the multiprocessor integrated circuit includes plural other processors ~~and said method further comprising:~~;

spawning a subtask from said first processor to another of said processors for sorting polygon edges in increasing minimum Y coordinate;

forming a queue of parallel tasks with said first processor; and

dispatching a parallel task from said queue to a next available other processor.